Claims

What is claimed is:

1. A method, comprising:

causing a carrier wafer to be fabricated to include a membrane on one side of said carrier wafer;

causing said membrane on said carrier wafer to bond to a surface of different, device wafer by a plurality of joints;

causing said joints and said device wafer to be isolated from exposure to etching chemicals; and

causing said carrier wafer to be selectively etched away to expose said membrane and to leave said membrane on said device wafer.

2. The method as in claim 1, wherein said carrier wafer includes a carrier semiconductor wafer and an insulator layer sandwiched between said carrier semiconductor wafer and said membrane, and wherein said selective etching of said carrier wafer includes:

causing a first etching process to be performed to remove at least a portion of said carrier semiconductor wafer to expose said insulator layer; and

causing a second etching process to be performed to remove said exposed portion of said insulator layer to expose a portion of said membrane.

3. The method as in claim 2, wherein said first etching process is a wet chemical etching process and said second etching process includes a plasma etching process.

4. The method as in claim 3, wherein said carrier semiconductor wafer includes silicon and said insulator layer includes a silicon-containing insulator material, wherein said first etching process uses a Tetramethylammonium hydroxide solution or a KOH solution.

5. The method as in claim 2, further comprising causing said device wafer to be formed from silicon, germanium, a III-V compound, or a II-VI compound.

6. The method as in claim 1, wherein said joints are indium bumps and are formed by:

causing a first set of indium bumps to be formed on said membrane on said carrier wafer and a second, corresponding set of indium bumps to be formed on said device wafer; and

causing said first set of indium bumps to hermetically bond to said second set of indium bumps to form joint indium bumps to engage said carrier wafer to said device wafer.

7. The method as in claim 6, wherein said hermetic bonding is formed by pressing said carrier and said device wafers against each other at an elevated temperature under a low pressure to directly bond said first and said second sets of indium bumps without applying an adhesive therebetween.

8. The method as in claim 6, further comprising causing a metalization layer to be formed between each indium bump and each of said carrier and said device wafers to have a gold contact layer in direct contact with each indium bump.

9. The method as in claim 8, wherein said metalization layer includes a layer of platinum (Pt) underneath said gold contact layer.

10. The method as in claim 1, wherein each joint is formed from an epoxy.

11. The method as in claim 1, further comprising:

causing a second carrier wafer to be fabricated to include a second membrane on one side of said second carrier wafer;

causing said second membrane on said carrier wafer to bond to said membrane by a plurality of second joints and to bond to said device wafer by a plurality of third joints;

causing said joints, said membrane, and said device wafer to be isolated from exposure to etching chemicals; and

causing said second carrier wafer to be selectively etched away to expose said second membrane and to leave said second membrane on said membrane and said device wafer.

12. A method, comprising:

causing a carrier wafer to be fabricated to include a support semiconductor wafer, a membrane on one side of said support semiconductor wafer, and an insulator layer sandwiched between said membrane and said support semiconductor wafer;

causing a first set of indium bumps to be formed on said membrane on said carrier wafer and a second, corresponding set of indium bumps to be formed on a separate device wafer;

causing said first set of indium bumps to hermetically bond to said second set of indium bumps to form joint indium bumps to engage said carrier wafer to said device wafer.;

causing said joint indium bumps and said device wafer to be isolated from exposure to etching chemicals; and

causing said carrier wafer to be selectively etched away to expose said membrane and to leave said membrane on said device wafer.

13. The method as in claim 12, further comprising causing a metalization layer to be formed between each indium bump and each of said carrier and said device wafers to have a gold contact layer in direct contact with each indium bump.

14. The method as in claim 13, wherein said metalization layer includes a layer of platinum (Pt) underneath said gold contact layer.

15. The method as in claim 12, wherein each set of indium bumps is formed by forming a layer of indium and patterning said layer of indium by a lift-off process.

16. The method as in claim 12, wherein said hermetic bonding is formed by pressing said carrier and said device wafers directly against each other at an elevated temperature under a vacuum condition to form a hermetic bond between said

first and said second sets of indium bumps without applying an adhesive therebetween.

17. The method as in claim 12, wherein said selective etching of said carrier wafer includes:

causing a wet etching process to be performed to remove at least a portion of said support semiconductor wafer to expose said insulator layer; and

causing a plasma etching process to be performed to remove said exposed portion of said insulator layer to expose a portion of said membrane.

18. The method as in claim 17, further comprising causing liquid etching drops to be applied subsequent to said plasma etching process to remove residue of said insulator layer.

19. The method as in claim 12, further comprising causing another plasma etching process to be formed to pattern said membrane by using a shadow mask.

20. The method as in claim 12, further comprising causing a layer of gold of to be deposited over each indium bump to prevent oxidation.